WHAT IS CLAIMED IS:

1. A method of reducing recess relief within an interconnect structure located in a layer of a semiconductor device, comprising:

conducting a fabrication process on an interconnect structure located in a dielectric layer that recesses said interconnect structure and forms a recessed substrate; and

conducting a recess reduction etch to remove a portion of said recessed substrate to reduce a relief of said recessed substrate.

2. The method as recited in Claim 1 wherein said recess reduction etch forms a substantially planar surface about said interconnect structure.

3. The method as recited in Claim 2 wherein said method further includes forming a metal-insulator-metal capacitor over said interconnect structure, subsequent to said subjecting.

4. The method as recited in Claim 1 wherein said recess reduction etch includes using a gas mixture comprising a gas compound containing fluorine, argon and nitrogen or hydrogen.

5. The method as recited in Claim 1 wherein said recess reduction etch is a plasma etch and a flow rate of said gas

compound containing fluorine is about 20 sccm, said argon is about 100 sccm and said nitrogen or said hydrogen is about 100 sccm.

6. The method as recited in Claim 4 wherein said gas compound is a fluorinated hydrocarbon compound.

7. The method as recited in Claim 6 wherein said fluorinated hydrocarbon compound is CH_2F_2.

8. The method as recited in Claim 1 wherein said recess reduction etch is conducted for about 10 seconds.

9. The method as recited in Claim 1 wherein said removing is conducted under substantially non-oxidizing conditions.

10. The method as recited in Claim 1 wherein a depth of said recess subsequent to said recess reduction etch ranges from about 3 nm to about zero nm.

11. A capacitor, comprising

a first conductive layer located on an interconnect structure formed in a dielectric layer, wherein a surface of said dielectric layer is substantially planar about said interconnect structure located in a dielectric layer;

a capacitor dielectric layer located over said first metal layer; and

a second conductive layer located over said capacitor dielectric layer.

12. The capacitor as recited in Claim 11 wherein a depth of a recess within a perimeter of said interconnect structure ranges from about 3.0 nm to about zero nm.

13. The capacitor as recited in Claim 11 a thickness of said first conductive layer ranges from about 20 nm to 100 nm.

14. The capacitor as recited in Claim 11 wherein said interconnect structure is a contact plug.

15. The capacitor as recited in Claim 14 wherein said contact plug comprises tungsten having a barrier layer between said tungsten and said dielectric layer .

16. A method of fabricating an integrated circuit, comprising:

forming transistors on a semiconductor substrate;

depositing dielectric layers over said transistors;

forming interconnect structures in said dielectric layers; and

forming a metal-insulator-metal capacitor on at least one of said interconnect structures, including:

conducting a fabrication process on an interconnect structure that recesses said interconnect structure and forms a recessed dielectric layer; and

conducting a recess reduction on said recessed dielectric layer, said recess reduction etch reducing said recessed substrate to form a substantially planar surface about said interconnect structure, prior to forming said metal-insulator-metal capacitor.

17. The method as recited in Claim 16 wherein said recess reduction etch includes using a gas mixture comprising a fluorinated hydrocarbon, argon and nitrogen or hydrogen.

18. The method as recited in Claim 17 wherein said recess reduction etch is a plasma etch and a flow rate of said fluorinated hydrocarbon is about 20 sccm, said argon is about 100 sccm and said nitrogen or said hydrogen is about 100 sccm.

19. The method as recited in Claim 17 wherein said recess reduction etch is conducted under substantially non-oxidizing conditions.

20. The method as recited in Claim 16 wherein a depth of said recess subsequent to said recess reduction etch ranges from about 3 nm to about zero nm.